SUPPRESSION OF CROSS DIFFUSION AND GATE DEPLETION

BACKGROUND OF THE INVENTION

The present invention relates to the suppression of cross diffusion and/or gate depletion in integrated circuit devices. More particularly, the present invention relates to a scheme for suppressing cross diffusion and gate depletion in a 6T SRAM cell.

Integrated circuit devices commonly employ a laminar or polycilicide structure composed of a polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. In many cases, the polycrystalline silicon film comprises an N+ polysilicon region doped with an N type impurity and a P+ polysilicon region doped with a P type impurity. The present inventors have recognized that many P+ and N+ dopant materials are subject to migration from a given polysilicon layer to another polysilicon layer, to an overlying conductive layer, or to another region of the given polysilicon layer. As a result, these opposite types of impurities are subject to cross diffusion. This cross diffusion can lead to performance degradation in the integrated circuit device.

Accordingly, there is a need for a scheme for suppressing cross diffusion of dopant materials between oppositely doped regions of polysilicon layers in integrated circuit devices.

BRIEF SUMMARY OF THE INVENTION

This need is met by the present invention wherein an ultrathin buried diffusion barrier layer (UBDBL) is formed over all or part of the doped polysilicon layer of a polycilicide structure composed of the polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride.

In accordance with one embodiment of the present invention, a memory cell is provided comprising a semiconductor substrate, a P well, an N well, an N type active region, a P type active region, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the

semiconductor substrate adjacent to the P well. The N type active region is defined in the P well and the P type active region is defined in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer over the N type active region and a P+ polysilicon layer over the P type active region. The diffusion barrier layer is formed in the polycilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

In accordance with another embodiment of the present invention, a memory cell is provide comprising a semiconductor substrate, a P well, an N well, an NMOS transistor, a PMOS transistor, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The P well is formed in the semiconductor substrate. The N well is formed in the semiconductor substrate. The NMOS transistor defines an N type active region in the P well. The PMOS transistor defining a P type active region in the N well. The isolation region is arranged to isolate the N type active region from the P type active region. The polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the NMOS transistor and a P+ polysilicon layer forming a portion of the PMOS transistor. The diffusion barrier layer is formed in the polycilicide gate electrode structure over a substantial portion of the polycrystalline silicon film between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film.

Preferably, the diffusion barrier layer comprises an ultrathin diffusion barrier layer and has a thickness of between about 5 Å and about 25 Å.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The P well formed in the semiconductor substrate. The N well formed is in the semiconductor substrate.

The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, an SRAM memory cell is provided comprising a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the N+ polysilicon layer and the P+ polysilicon layer.

In accordance with yet another embodiment of the present invention, a memory cell array is provided comprising a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor

substrate, a P well, an N well, a flip flop, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. The isolation region is arranged to isolate the N type active region from the P type active region. The polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a computer system is provided including a microprocessor in communication with a memory cell array via a data communication path. The memory cell array comprises a plurality of SRAM cells arranged in rows and columns. Each cell of the array is connected to a word line and to a pair of bit lines and comprises a semiconductor substrate, a P well, an N well, a flip flop, an isolation region, a polycilicide gate electrode structure, and a diffusion barrier layer. The flip-flop is formed by two access transistors and a pair of cross coupled inverters. Each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor. The pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well. An isolation region is arranged to isolate the N type active region from the P type active region. A polycilicide gate electrode structure is composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film. The polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor. The diffusion barrier layer is formed in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating an SRAM memory cell is provided. Recited in terms of physical location, as opposed to chronological order of processing, the method comprises the steps of (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) forming a P type active region of a pull-up transistor in the N well, (v) forming a gate oxide layer and a conductive gate of the pull-up transistor over the P type active region, (vi) forming an N type active region of a pull-down transistor in the P well; (vii) forming a gate oxide layer and a conductive gate of the pull-down transistor over the N type active region, (viii) forming an isolation region between the N type active region and the P type active region, (ix) forming a polycrystalline silicon film over the pull-down transistor and the pull-up transistor, (x) doping selectively the polycrystalline silicon film to form an N+ polysilicon layer over the pull-down transistor and a P+ polysilicon layer over the pull-up transistor; (xi) forming a diffusion barrier layer over a substantial portion of the polycrystalline silicon film, and (xii) forming a metal, metal silicide, or metal nitride film over the doped polycrystalline silicon film and the diffusion barrier layer. The diffusion barrier layer is formed by selective chemical oxidation of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a memory cell array by arranging a plurality of the SRAM cells in rows and columns and connecting each SRAM cell of the array to a word line and to a pair of bit lines is provided. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying

metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, and (vii) forming a diffusion barrier layer in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

In accordance with yet another embodiment of the present invention, a method of fabricating a computer system is provided. The computer system is fabricated by arranging a microprocessor in communication with a memory cell array via a data communication path and fabricating the memory cell array by arranging a plurality of the SRAM cells in rows and columns and connecting each SRAM cell of the array to a word line and to a pair of bit lines. Recited in terms of physical location, as opposed to chronological order of processing, each of the SRAM cells is fabricated by (i) providing a semiconductor substrate, (ii) forming a P well in the semiconductor substrate, (iii) forming an N well in the semiconductor substrate, (iv) providing a flip-flop including two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein the pull-up transistor defines a P type active region in the N well and the pull-down transistor defines an N type active region in the P well, (v) arranging an isolation region to isolate the N type active region from the P type active region, (vi) providing a polycilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein the polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of the pull-down transistor and a P+ polysilicon layer forming a portion of the pull-up transistor, (vii) forming a diffusion barrier layer in the polycilicide gate electrode structure between the polycrystalline silicon film and the metal, metal silicide, or metal nitride film over a substantial portion of the polycrystalline silicon film.

Accordingly, it is an object of the present invention to provide an integrated circuit and an integrated circuit fabrication scheme where cross diffusion of dopant materials between oppositely doped regions of polysilicon layers is suppressed. Other objects of the present invention will be apparent in light of the description of the invention embodied herein.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The following detailed description of the preferred embodiments of the present invention can be best understood when read in conjunction with the following drawings, where like structure is indicated with like reference numerals and in which:

Fig. 1 is a schematic circuit diagram of a six transistor SRAM cell according to the present invention;

Fig. 2 is a cross-sectional view of a CMOS structure used in the SRAM cell illustrated in Fig. 1;

Fig. 3 is an illustration of an SRAM cell array according to the present invention;

Fig. 4 is a schematic block diagram of a computer system according to the present invention; and

Figs. 5-7 are schematic illustrations of schemes for suppressing cross diffusion according to the present invention.

DETAILED DESCRIPTION

Initially, the present invention may be illustrated in the context of a six transistor static random access memory cell (See Figs. 1 and 2). Most metal oxide semiconductor (MOS) static random access memories (SRAMs) have in common a basic cell consisting of two transistors and two load elements in a flip-flop configuration, together with two access transistors. For example, Fig. 1 presents a schematic circuit diagram of a six transistor (6T) SRAM cell. The SRAM cell **1** includes two N type MOS (NMOS) transistors **N1** and **N2** coupled between V_{SS} and nodes A and B, respectively. Nodes A and B are further coupled to V_{DD} by pull up P type MOS (PMOS) transistors **P1** and **P2**, respectively. Node A is further coupled to the gates of transistors P2 and **N2** and node B is similarly coupled to the gates of transistors **P1** and **N1**. V_{SS} is typically ground and V_{DD} is typically 3.3 volts or 5.0 volts.

Information is stored in SRAM cell **1** in the form of voltage levels in the flip-flop formed by the two cross-coupled inverters 2 and 3 formed by transistors **P1**, **N1** and **P2**, **N2**, respectively. Specifically, when node **A** is at a logic low state, i.e., when the voltage of node **A** is approximately equal to V_{SS}, transistor **P2** is on and transistor **N2** is off. When transistor **P2** is on and transistor **N2** is off, node **B** is at a logic high state, i.e., the voltage of node **B** is pulled up to approximately V_{DD}. When node **B** is at a logic high state, transistor **P1** is off and transistor **N1** is on. When transistor **P1** is off and transistor **N1** is on, node **A** is at a logic low state. In this manner, SRAM cell **1** remains in a latched state.

Nodes **A** and **B** are further coupled to bit lines **BL** by NMOS access transistors **N3** and **N4**, respectively. The gates of transistors **N3** and **N4** are coupled to a word line **WL** to enable conventional read and write operations.

Fig. 2 is a cross-sectional view of a conventional complimentary metal oxide semiconductor (CMOS) structure **4** used in conventional 6T SRAM cells like the one described with reference to Fig. 1. As is shown in Fig. 2, a P well **5** and an N well **6** are formed adjacent to each other in a semiconductor substrate **7**. Formed at the surface of substrate **7** are isolation regions **8**, i.e., shallow trench isolation regions, field oxide regions, etc. Formed above P well **5** and N well **6** are gate oxide layers **9**. Formed over gate oxide layers **9** are conductive gates **10** of an NMOS transistor **11** and a PMOS transistor **12**. The PMOS transistor **12** may be a pull up transistor of an SRAM cell. The NMOS transistor **11** may be a pull down/access transistor of an SRAM cell. The CMOS structure **4** includes an N type active region defined in the P well **5** of the NMOS transistor **11** and a P type active region defined in the N well **6** of the PMOS transistor **12**. The isolation regions **8** are defined between the N type and P type active regions of the CMOS structure and isolate electrically the N type and P type active regions of the substrate **7** from each other.

As is shown in Fig. 2, N+ source/drain regions **13** of the NMOS transistor **11** include N+ heavily doped source/drain regions **15** laterally aligned (self aligned) to sidewall spacers **16**. Similarly, P type source/drain regions **17** of the PMOS transistor **12** include P+ heavily doped source/drain regions **19** laterally aligned (self aligned) to sidewall spacers **16**.

The gate electrode structure of the CMOS structure **4** is constructed to have a laminar or polycilicide structure composed of a polycrystalline silicon film and an overlying film of a metal, metal silicide, or metal nitride. Specifically, the polycrystalline silicon film comprises an N+ polysilicon layer **21** formed over the NMOS transistor **11** and a P+ polysilicon layer **22** formed over the PMOS transistor **12**. Each of the polysilicon layers **21**, **22** typically provide a connection to a transistor gate. The N+ polysilicon layer **21** is doped with an N type impurity such as arsenic (As) or phosphorous P31. The P+ polysilicon layer **22** is doped with an N type impurity such as boron (B). The overlying metal, metal silicide, or metal nitride layer **24** is typically formed of a tungsten silicide (WSi_X: x=**2**, for example) and contributes to an accelerated signal transmission rate because the specific resistance of the metal, metal silicide, or metal nitride layer **24** is lower than that of the polycrystalline silicon layers **21**, **22**. The metal, metal silicide, or metal nitride layer **24** may be made of not only WSi_X but also molybdenum silicide $MoSi_X$, titanium silicide $TiSi_X$, tantalum silicide $TaSi_X$, cobalt silicide, nitrides of these metals, etc. An insulating capping layer **26** is formed over the WSi_X layer **24** and is typically formed of silicon dioxide or silicon nitride.

P+ and N+ dopant materials like arsenic and boron are subject to migration from a given portion of a polysilicon layer to another portion of the polysilicon layer or another polysilicon layer where the layers are covered by a metal, metal silicide, or metal nitride layer. Specifically, the dopant materials will migrate from the originating polysilicon layer, through the overlying metal, metal silicide, or metal nitride layer, to the other region of the polysilicon layer or another polysilicon layer. This migration or cross-diffusion results in depletion of the doped polysilicon layers. According to the present invention, an ultrathin buried diffusion barrier layer (UBDBL) **28** is formed over the P+ polysilicon layer **22** illustrated in Fig. 2 to address this problem. The UBDBL layer **28** also prevents poly depletion by not allowing N+ dopants to counter dope P+ dopants in the P+ polysilicon layer 22 or other P+ polysilicon region.

The UBDBL layer **28**, which may, for example, be a thin silicon dioxide layer, a thin silicon nitride layer, or another form of barrier layer, suppresses the migration of N+ dopant material from the N+ polysilicon layer **21** into the P+ polysilicon layer **22**. Specifically, the N+

dopant material, which may be arsenic, moves relatively quickly in the overlying metal, metal silicide, or metal nitride layer **24** but will not readily migrate through the UBDBL layer **28**. Thus, the UBDBL layer **28** suppresses undesirable cross-diffusion of the N+ dopant into the associated P+ polysilicon layer **22**. Similarly, any P+ dopant material (e.g., boron) in the UBDBL layer **28** will not readily migrate out of the UBDBL layer **28**. Thus, the UBDBL layer **28** suppresses undesirable cross-diffusion of the P+ dopant into the associated N+ polysilicon layer **21**. In this manner, the UBDBL layer **28** forms a significant barrier to migration of the N+ dopant and the P+ dopant and, as such, may be used to suppress cross-diffusion.

The thickness of the UBDBL layer **28** is selected to minimize its impact on device performance. Specifically, it is noted that, throughout the various embodiments of the present invention, electrical connections are established between specific electrode structures and the associated polysilicon layers of the present invention by means of capacitive coupling through the UBDBL layer **28**. Further, UBDBL layer is preferably only utilized over doped polysilicon layers of pull-up and pull-down devices because the operational speed of these devices is not as critical to SRAM performance as is, for example, the operational speed of SRAM periphery transistors. Typically, the thickness of the UBDBL **28** is between about 10 Å and 15 Å. However, it is noted that UBDBL thicknesses as low as 3 Å and as high as 125 Å may be employed according to the present invention. By comparison, the polysilicon layers **21**, **22** typically have thicknesses in the range of between about 500 Å and 4000 Å and the metal, metal silicide, or metal nitride layer **24** typically has a thicknesses of about 500 Å to about 1500 Å. The UBDBL **28** may be formed, for example, through convention chemical oxidation processes, including oxidation in dilute H_2O_2, furnace oxidation, remote plasma oxidation, etc.

The UBDBL layer **28** is particularly advantageous where the N+ polysilicon layer **21** is doped with a material that migrates in the metal, metal silicide, or metal nitride layer **24**. More specifically, the UBDBL layer **28** is particularly advantageous where the N+ polysilicon layer **21** is doped with arsenic (As), the P+ polysilicon layer **22** is doped with boron (B), and the overlying metal, metal silicide, or metal nitride layer **24** is a WSi_X metal silicide layer.

It is noted that only a portion of the polysilicon layers **21**, **22**, the metal, metal silicide, or metal nitride layer **24**, the capping layer **26**, and the UBDBL layer **28** are illustrated in Fig. 2 because the manner in which they are patterned and configured is largely dependent upon the design constraints of the specific integrated circuit structure and is outside the scope of the present invention. The present invention relates primarily to the interposition of the UBDBL layer **28** between the P+ polysilicon layer **22** and the metal, metal silicide, or metal nitride layer **24** to suppress the cross diffusion of the N+ dopant from the into the P+ polysilicon layer **22**.

Referring to Fig. 3, an SRAM cell array **50** embodying the present invention is illustrated. The array **50** includes a number of SRAM cells **52** arranged in rows and columns. Each cell **52** is connected to a word line WL and to a pair of bit lines BL. A computer system **60** including a microprocessor **61** in communication with an SRAM cell array **50** of the present invention is illustrated in Fig. 4. The computer system **60** further includes ROM **62**, mass memory **64**, peripheral devices **66**, and I/O devices **68**, all in communication with the microprocessor **62** via a data bus **65** or another suitable data communication path.

Referring now to Figs. 5-7, although the present invention is well-suited for use in the context of the 6T SRAM cell described with reference to Figs. 1-4, it is noted that the present invention is also more generally applicable to integrated circuit structures where cross diffusion and gate depletion are a concern. Accordingly, the present invention is also described herein with reference to Figs. 5-7, which provide a more general illustration of integrated circuit structures where cross diffusion and gate depletion are a concern.

In the embodiment illustrated in Fig. 5, the UBDBL **28** and the polycilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the P+ polysilicon layer **22** between the P+ polysilicon layer **22** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the N+ polysilicon layer **21**. Stated differently, the UBDBL **28** is arranged such that the metal, metal silicide, or metal nitride film **24** is in direct contact with the N+ polysilicon layer **21** and defines an N type common boundary with the N+ polysilicon layer **21** that is significantly larger than any P type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the P+ polysilicon

layer **22**. The UBDBL **28** may be formed over the entire extent of that portion of the P+ polysilicon layer **22** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** to the overlying metal, metal silicide, or metal nitride film **24** is significantly impeded by the UBDBL **28**. Although dopants from the N+ polysilicon layer **21** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and P+ poly gate depletion are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the P+ polysilicon layer **22**.

Similarly, in the embodiment illustrated in Fig. 6, the UBDBL **28** and the polycilicide gate electrode structure are arranged such that the UBDBL **28** is formed over a substantial portion of the N+ polysilicon layer **21** between the N+ polysilicon layer **21** and the metal, metal silicide, or metal nitride film **24** and does not extend over a substantial portion of the P+ polysilicon layer **22**. Stated differently, the UBDBL **28** is arranged such that the metal, metal silicide, or metal nitride film **24** is in direct contact with the P+ polysilicon layer **22** and defines an P type common boundary with the P+ polysilicon layer **22** that is significantly larger than any N type common boundary defined by the metal, metal silicide, or metal nitride film **24** and the N+ polysilicon layer **21**. The UBDBL **28** may be formed over the entire extent of that portion of the N+ polysilicon layer **21** that is overcoated by the metal, metal silicide, or metal nitride film **24**. In this manner, migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal nitride film **26** is significantly impeded by the UBDBL **28**. Although dopants from the P+ polysilicon layer **22** enter the overlying metal, metal silicide, or metal nitride film **24**, cross diffusion and N+ poly gate depletion are suppressed because these dopants, present in the overlying metal, metal silicide, or metal nitride film **24**, cannot cross the UBDBL **28** and enter the N+ polysilicon layer **21**.

Finally, in the embodiment illustrated in Fig. 7, the UBDBL **28** is formed in the polycilicide gate electrode structure over the N+ polysilicon layer **21** and the P+ polysilicon layer **22**. In this manner, migration of P+ dopants from the P+ polysilicon layer **22** and migration of N+ dopants from the N+ polysilicon layer **21** to the overlying metal, metal silicide, or metal

nitride film **24** is significantly impeded by the UBDBL **28**. Cross diffusion and gate depletion are suppressed because the dopants cannot cross the UBDBL **28** and enter the opposite polysilicon layer.

The various layers, regions, and structures of the device according to the present invention may be formed by utilizing conventional semiconductor device fabrication techniques. The selection of these specific techniques may vary from application to application and, with the exception of the fabrication steps outlined herein, is not the subject of the present invention. Referring to Fig. 2, an SRAM memory cell according to the present invention may be fabricated by providing a semiconductor substrate **7** and forming the P well **5** and the N well **6** in the semiconductor substrate **7**. The P type active region of the pull-up transistor **12** is formed in the N well **6** and the gate oxide layer **9** and the conductive gate **10** of the pull-up transistor **12** are formed over the P type active region. The N type active region of the pull-down transistor **11** is formed in the P well **5** and the gate oxide layer **9** and the conductive gate **10** of the pull-down transistor **11** are formed over the N type active region. The isolation regions **8** are formed between the N type active region and the P type active region. The polycrystalline silicon film is formed over the pull-down transistor and the pull-up transistor and is doped selectively to form the N+ polysilicon layer **21** over the pull-down transistor **11** and the P+ polysilicon layer **22** over the pull-up transistor **12**. The UBDBL or diffusion barrier layer **28** is formed over the entire polycrystalline silicon, or at least a substantial portion thereof, and the metal, metal silicide, or metal nitride film **24** is formed over the doped polycrystalline silicon film and the diffusion barrier layer **28**. Preferably, the diffusion barrier layer **28** is formed by selective chemical oxidation of the polycrystalline silicon film or rapid plasma nitridation.

To fabricate the memory cell array **50** of Fig. 3, the SRAM cells **52** are arranged in rows and columns and each SRAM cell **52** of the array **50** is connected to a word line WL and to a pair of bit lines BL. To fabricate the computer system **60**, the microprocessor **61** is arranged in communication with the memory cell array **50** via a data communication path **65**.

Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from

the scope of the invention defined in the appended claims. More specifically, although some aspects of the present invention are identified herein as preferred or particularly advantageous, it is contemplated that the present invention is not necessarily limited to these preferred aspects of the invention.

What is claimed is: